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Description

System And Method Of Digitally Testing An Analog Driver Circuit

BACKGROUND OF INVENTION

[0001] The present invention relates to testing analog driver circuitry using digital scan-based test methodologies such as level-sensitive scan design (LSSD) or any flip-flop based scan technique. Digital scan-based test methodologies typically define a number of Shift Register Latches ("SRLs") that are electrically coupled in series and may be set deterministically by digital test equipment, such that application of a test vector defines the state of the device under test. Separate SRLs may be driven by outputs of the device under test. After the test is complete, the test equipment scans the output vector out of the SRLs and compares it against an expected output vector. SRLs which sense the output of a circuit under test can only interpret digital states and cannot interpret an analog state. Digital scan-based testing methodologies are well known

in the art, and in particular, the implementation of a digital scan architecture into a design, the generation of patterns for testing the design, and the stimulation and observation of circuits within the design is well known. For example, see US Patent no. 4,298,980, entitled LSI Circuitry conforming to level sensitive scan design (LSSD) rules and method of testing same, by Hajdu et al. Use of SRLs for scan-based testing is well known to those skilled in the art. For example, see Miron Abramovici et al., "Digital Systems Testing and Testable Design", IEEE PRESS, Ch. 9.3-9.9, 1990.

[0002] Analog driver circuitry typically requires functional testing to ascertain whether the driver functions as expected. As technology integration has become more complex, for example the integration of analog and digital circuits in the same design, testing of analog circuitry has become more difficult and expensive. There are several disadvantages associated with functional testing, such as: (1) it is more difficult to debug a functional test of a large analog/digital circuit as compared to digital scan-based logical paths; (2) it is more expensive to package a device for functional test than to test the device at the wafer level; and (3) more generally, development cost, difficult debugging and the

high cost of test hardware make functional testing unappealing. For example, as operating voltages continue to decrease (e.g. 1.2V and below) and as the precision of digital-to-analog converters (DACs) increase, it is extremely difficult to digitally test the least significant bits (LSBs) of DACs where the DAC current output is converted to a voltage with a very low impedance (e.g. 50 ohms). For illustrative purposes, consider a seven-bit DAC which is operated at 1.2V. The output differential amplitude of the DAC for the LSB would be 9mV at an output termination impedance of 50 ohms (1.2V / 127). The offset voltage of a differential receiver is typically much larger than the LSB of the DAC, thus making the receiver's interpretation of the driver output unreliable. It is therefore desirable to provide a system and apparatus which is capable of testing an analog driver circuit of a mixed-signal design at the wafer-level, avoiding the extra cost associated with analog test equipment or on-chip analog BIST circuits.

[0003] See the following US patents for examples of analog test equipment, which are typically expensive and add to circuit test time: US Patent no. 5,610,530, entitled Analog interconnect testing, by Whetsel; US Patent no. 5,481,471, entitled Mixed signal integrated circuit architecture and

test methodology, by Naglestad et al.; US Patent no. 5,107,208, entitled System for partitioning and testing submodule circuits of an integrated circuit, by Lee; and US Patent no. 6,011,387, entitled Analog autonomous test bus framework for testing integrated circuits on a printed circuit board, by Lee. See the following references for examples of analog BIST circuits implemented on chip, which are expensive in design time and chip area: US Patent no. 5,861,774, entitled Apparatus and method for automated testing of a programmable analog gain stage, by Blumenthal; and Karim Arabi, Bozena Kaminska, and Janusz Rzeszut, "BIST for D/A and A/D converters," IEEE Design & Test of Computers v. 13 n. 4 Winter 1996, pp. 40-49.

BRIEF DESCRIPTION OF DRAWINGS

[0004] FIG. 1 is a diagram illustrating a scan-compatible analog differential driver circuit according to the present invention.

[0005] FIG. 2 is a diagram illustrating a differential driver circuit according to the present invention.

[0006] FIG. 3 is a diagram illustrating a programmable termination impedance network according to the present invention.

[0007] FIG. 4 is a diagram illustrating a differential receiver circuit with built-in offset voltage according to the present invention.

[0008] FIG. 5 is a diagram illustrating a LSSD test mode control circuit according to the present invention.

[0009] FIG. 6 is a diagram illustrating a method of digitally testing a scan-compatible analog differential driver circuit according to the present invention.

BRIEF DESCRIPTION OF SEQUENCES

[0010] The present inventors believe that the prior art has at least the following drawbacks:

[0011] An object of the invention is to digitally test an analog driver circuit.

[0012] Another object of the invention is to digitally test an analog driver circuit using a scan-based testing methodology.

[0013] Another object of the invention is to digitally stimulate and observe an analog driver circuit from shift-register latches.

[0014] Another object of the invention is to digitally stimulate and observe the least-significant-bit of an analog driver circuit by skewing the output termination impedance of an analog driver circuit.

[0015] Another object of the invention is to digitally test an ana-

log driver circuit by converting the differential output of an analog driver circuit into a common mode signal by skewing the output termination impedance of the analog driver circuit, detecting the skewed signal with a differential receiver circuit and converting the detected skewed signal into a single-ended signal for observation.

[0016] Another object of the invention is to digitally test an analog driver circuit by detecting a skewed signal with a differential receiver circuit, wherein the receiver circuit incorporates a comparator circuit with built-in offset voltage for reliably detecting the state of the driver circuit.

[0017] Another object of the invention is to either skew or match the output termination impedance of a differential driver circuit in response to a test enable signal, wherein the impedance is skewed when the test enable signal is active and matched otherwise.

[0018] Another object of the invention is to receive a skewed common mode signal with a differential receiver circuit and convert the detected signal into a single-ended signal in response to a test enable signal.

[0019] Another object of the invention is to disable an up-channel receiver, enable the up-channel receiver for up-channel signaling, or enable the up-channel receiver for

digital scan-based testing, all in response to a test enable signal.

DETAILED DESCRIPTION

[0020] Figure 1 illustrates the preferred embodiment of the invention. Scan-compatible analog differential driver circuit 100 comprises differential driver 110, programmable termination impedance network 120, up-channel receiver 130 and LSSD test mode control circuit 140. Differential driver 110 may be any differential driver circuit incorporating a Digital-to-Analog Converter (DAC) and having large dynamic gain. In the preferred embodiment, driver 110 is a high-speed (e.g. 6 Gbps or higher) differential finite-impulse-response (FIR) I/O driver with large dynamic gain as described in US Patent no. 6,680,681, entitled High Speed FIR Transmitter, by Hsu et al., the subject matter of which is hereby incorporated by reference in its entirety. Data inputs AP and AN to differential driver 110 represent differential data inputs.

[0021] Programmable termination impedance network 120 sets the termination impedance at differential output nodes ZP and ZN. During digital scan test mode (e.g. LSSD testing), programmable termination impedance network 120 skews the termination impedance at differential output nodes ZP

and ZN in response to signals RESCTRL_P<5:0> and RESCTRL_N<5:0>. When the termination impedance is skewed at differential output nodes ZP and ZN, the differential output of driver 110 (DOP and DON) is skewed, and thus, up-channel receiver 130 is capable of detecting the full dynamic range of driver 110. Skewing the output termination impedance serves to covert DOP and DON into a common-mode signal. During normal operation, programmable termination impedance network 120 programs the termination impedance at output nodes ZP and ZN in response to signals RESCTRL_P<5:0> and RESCTRL_N<5:0> to the appropriate termination resistance for optimum transmission (e.g. matched 50 Ohm impedance at ZP and ZN).

[0022] Up-channel receiver 130 may be any receiver circuit with voltage offset such that when inputs to the receiver are equal, the receiver reliably outputs a low voltage. Alternatively, up-channel receiver 130 may incorporate hysteresis for improved noise immunity during up-channel signaling. Up-channel signaling is well known in the art. For example, see US Patent Application No. 10/604025, entitled Data Transceiver And method for Equalizing The Data Eye of a Differential Input Data Signal, assigned to IBM Corpo-

ration. In the preferred embodiment, up-channel receiver 130 is a differential receiver with a built-in offset voltage and hysteresis, and is capable of receiving signals transmitted up-channel (i.e. in the opposite direction as the data being transmitted). Such receivers are incorporated in high speed serializer-deserializer (SERDES) circuit designs for up-channel signaling, and thus, circuit area may be minimized when an up-channel receiver with hysteresis is already present in a design. Up-channel receiver 130 is used to complete the observation path from the output of driver 110 to a SRL or a Primary output during digital scan-based testing. During normal operation, up-channel receiver 130 may sense a signal as low as 70mv. However, there will be some ambiguity at these low levels. Since digital scan-based test mode requires deterministic results of either a logic '1' or '0' without 'x' propagation, the area of ambiguity must be removed. This is accomplished by changing the characteristics of up-channel receiver 130 during test mode. When up-channel receiver 130 is placed in test mode by LSSD_EN, offset and gain characteristics of the receiver are changed such that the receiver now requires a 150mv signal or the output will result in a '0'. This increased voltage offset (~70mv) guarantees that

when all DACs are turned off in driver 110, there will be a logic '0' output from up-channel receiver 130 at node Z. Additionally, by skewing the termination impedance at nodes ZP and ZN during test mode, the LSB of driver 110 can be observed as a logic '1' at the output of up-channel receiver 130.

[0023] LSSD Test Mode Control Block 140 enables scan-compatible driver circuit 100 of Figure 1 for digital testing by overriding the nominal control signals RESCTRL_P<5:0> and RESCTRL_N<5:0> and by overriding the nominal segment control vector SEG_DISABLE<7:0>. By overriding the nominal control signals RESCTRL_P<5:0> and RESCTRL_N<5:0>, the output termination impedance at nodes ZP and ZN may be skewed, thus allowing observation of the LSB of the differential driver. By overriding the nominal segment control vector SEG_DISABLE<7:0>, each segment of differential driver 110 may be tested one at a time, thus assuring the LSBs of the driver are effectively tested for faults. These signals are overridden in response to LSSD_EN. In the preferred embodiment, LSSD_EN signal is a primary input. A detailed description of the aforementioned signals follows.

[0024] During digital test mode, up-channel receiver 130 is en-

abled for digital testing by LSSD_EN and powered on by PDWN. Up-channel receiver 130 functions as an Analog-to-Digital Converter (ADC) and is capable of passing a digital value Z, which represents the output of differential driver 110, to a shift register latch ("SRL") which is observable during digital testing. During digital test mode, the termination impedance is skewed, thus enabling up-channel receiver 130 to detect the full dynamic range of differential driver 110 even though the least-significant-bits (LSBs) effect a much smaller change than up-channel receiver 130 could detect during normal operation. Detecting the LSB of differential driver 110 enables the digital-to-analog converters (DACs) residing within differential driver 110 to be fully digitally modeled (e.g. as a number of n-bit OR gates), thus enabling an automatic test pattern generator to generate test patterns for the entire DAC circuit. If the termination impedance is not skewed, the voltage offset of up-channel receiver 130 will be much larger than the LSB of driver 110, making the receiver's interpretation of the output of driver 110 unreliable. By skewing the termination impedance, the LSB of the DAC may be tested using a scan-based digital test methodology. During normal operation, up-channel re-

ceiver 130 is taken out of digital test mode by disabling LSSD_EN. Additionally, up-channel receiver 130 may be powered down by activating PDWN or may remain powered on by leaving PDWN deactivated.

[0025] Figure 2 illustrates in further detail differential driver 110 of Figure 1. Finite Impulse Response (FIR) latches 210 store differential data inputs AP<3:0> and AN<3:0> and present AP<3:0> and AN<3:0> to driver logic 220. XNOR circuits 230 may invert AP<x:0> and AN<x:0> in response to data polarity signal TX_POLARITY<3:0> or may disable AP<x:0> and AN<x:0> in response to data disable signal TAPDIS0/2/3. Buffer circuits 240 buffer the output of XNOR circuits 230. Predriver circuits 250 amplify the differential data signals. Each predriver circuit contains one or more preamplifiers ("segments"). As illustrated in Figure 2, predriver circuit 250A comprises one segment, predriver circuit 250B comprises four segments, predriver circuit 250C comprises two segments, and predriver circuit 250D comprises one segment. If a differential data bit is preamplified by more than one segment, driver output stages 260 are paralled per segment for that differential data bit. As illustrated in Figure 2, predriver circuit 250B contains four segments, and therefore, driver

260B will have four parallel differential inputs from each of the four segments contained in predriver circuit 250B.

[0026] Each paralleled output stage has a separate predriver, driven from the same driver logic (XNOR circuits 220 and buffer circuits 240). The number of segments per differential data bit determines the drive strength for that differential data bit. The more segments, the higher the drive strength for the programmed current. Any segment may be disabled via the SEG_DISABLE<x:0> signal. The output drive strength of output drivers 260A-260D is set by current DAC (IDAC) circuit 270. IDAC circuit 270 comprises IDACs 270A-270D. The value of each IDAC 270A-270D is set by TX_COEFFX<x:0>. As illustrated in Figure 2, the value of IDAC 270A is determined by TX_COEFF3<3:0>. The range of the current reference (IREF) for each IDAC 270A-270D is set by the output of power DAC 280, which is controlled by TX_POWER<6:0>. The differential output of drivers 260A-260D are tied together at differential output nodes ZP and ZN to form the final pair of output signals, DOP and DON. During digital testing, signals TX_COEFFX<n:0>, TAPDIS0/2/3, TX_POWER<6:0>, TX_POLARITY<3:0>, AP<3:0>, and AN<3:0> are supplied from SRLs, thus making the differential driver digitally

testable.

[0027] Figure 3 illustrates in further detail programmable termination impedance network 120 of Figure 1. Programmable termination impedance network 300, which corresponds to programmable termination impedance network 120 of Figure 1, comprises programmable resistor circuits 310 and 320. Resistor circuit 310 comprises a number of resistor components 312 and number of transistor switches 314, wherein one transistor of transistor switches 314 is electrically coupled in series with one resistor of resistor components 312. Resistor circuit 320 also comprises a number of resistor components 322 and number of transistor switches 324, wherein one transistor of transistor switches 324 is electrically coupled in series with one resistor from resistor components 322. When a particular resistor is switched into the resistor network by a transistor, that resistor component is electrically coupled in parallel with all other resistors that are also switched into the network. When a particular resistor is switched out of the resistor network, it is electrically isolated from the impedance network. In the preferred embodiment, resistor circuits 310 and 320 each comprise six resistors, the value of which are as follows: Rp1 = 53.65 Ohms, Rp2 =

71.15 Ohms, Rp3 = 144.35 Ohms, Rp4 = 286.95 Ohms, Rp5 = 554 Ohms, and Rp6 = 3001 Ohms, where: Rn1 = Rp1, Rn2 = Rp2, Rn3 = Rp3, Rn4 = Rp4, Rn5 = Rp5, and Rn6 = Rp6. In the preferred embodiment, transistor switches 314 and 324 comprise six p-FET transistors.

[0028] Resistor circuit 310 provides termination impedance to output node ZP of differential driver 110 of Figure 1 and resistor circuit 320 provides termination impedance to output node ZN of differential driver 110 of Figure 1. Control signal RESCTRL_P<5:0> programs resistor circuit 310 and control signal RESCTRL_N<5:0> programs resistor circuit 320 by either activating or deactivating the transistor electrically in series with a certain resistor. Both RESCTRL_P and RESCTRL_N are determined by LSSD test mode control block 140 of Figure 1. RESCTRL_P and RESCTRL_N switch in or out resistor components within resistor circuits 310 and 320, thus programming the termination impedance at nodes ZP and ZN, respectively. During digital scan test mode, the termination impedance provided by resistor circuits 310 and 320 is programmed so that the termination impedance of programmable termination impedance network 300 is skewed at nodes ZP and ZN. For example, the termination impedance at node

ZP, determined by those resistors in resistor circuit 310 which are switched in to the network by corresponding transistor switches 314 and those that are not, may be programmed to 54 Ohms while the termination impedance at node ZN is programmed to 554 Ohms. This occurs when RESCTRL_P<5:0> = "011111" and RESCTRL_N<5:0> = "111101". When the termination impedance is skewed in such a manner, the differential output of driver 110 in Figure 1 is converted to a common mode signal because the differential signal at node ZN of the driver will be 10x larger than the same signal at node ZP, thus resulting in a differential-to-common mode gain of 5x.

[0029] During normal operation, signals RESCTRL_P<5:0> and RESCTRL_N<5:0> program transistor switches 314 and 324 so that the output termination impedance at nodes ZP and ZN match. This occurs when RESCTRL_P<5:0> = RESCTRL_N<5:0>. For illustrative purposes, consider a differential driver that comprises a seven-bit DAC where: the LSB of the 7 bit DAC = 1.2V/127 = 9 mV in terms of driver output differential amplitude at 50ohms and 90mV at 500 ohms. LSB of 4/5/6 bit DAC = 19 mV of Driver output differential amplitude at 50ohms and 190mV at

500 ohms. Up-channel receiver 130 of Figure 1 is capable of detecting these amplitudes for a termination resistance of 500 ohms, but can not detect these amplitudes at 50 ohms, because the amplitude is less than the receiver's offset voltage. As DACs are designed more precisely, the LSB will become smaller and more difficult to detect in a digital test framework. A number of resistor/transistor combinations as well as resistor values are possible and within the scope of the invention.

[0030] Figure 4 illustrates in further detail up-channel receiver 400, which corresponds to up-channel receiver 130 of Figure 1. Up-channel receiver 400 comprises a hysteresis comparator circuit 402 and a common level shifter 404. Common level shifter 404 provides transition from an analog power supply domain ("VTT") to a digital power supply domain ("VDD"). Level shifters are well known to those skilled in the art, and therefore, no further description is necessary. Hysteresis comparator circuit 402 comprises reference current source 406, first built-in offset voltage comparator 408, second built-in offset voltage comparator 410, differential amplifier circuit 412, and output stage 414. Reference current source 406 comprises p-fet transistor TPL2 and n-fet transistor T1 and

generates reference current IOREF. Current sources are well known to those skilled in the art, and therefore, no further description is necessary.

[0031] First built-in offset voltage comparator 408 comprises p-fet transistors TEL, TPL, and TNL. The comparator has a built-in offset voltage ("Vth-"). The value of Vth- is dependent upon the ratio of TNL to TPL as well as the biasing current IBIAS. In general, the higher the ratio or higher the biasing current, the higher Vth- becomes. As previously stated, this offset voltage provides improved noise immunity. Without this offset voltage, a comparator would output a high when VINP > VINN, output a low when VINP < VINN, and output an unknown value when VINP=VINN. Such a comparator has zero noise margin due to the fact that a minimal amount of noise triggers a response. First built-in offset voltage comparator 408 addresses Low to High transitions at VINP and VINN. VINP corresponds to DOP and VINN corresponds to DON as illustrated in Figure 1, where DOP and DON represent the differential output of differential driver 110 of Figure 1.

[0032] Second built-in offset voltage comparator 410 comprises p-fet transistors TER, TPR, and TNR. The comparator has a built-in offset voltage ("Vth+"). The value of Vth+ is de-

pendent upon the ratio of TNR to TPR as well as the biasing current IBIAS. In general, the higher the ratio or higher the biasing current, the higher Vth+ becomes. As previously stated, this offset voltage provides improved noise immunity. Second built-in offset voltage comparator 410 addresses High to Low transitions at the inputs VINP and VINN. Differential amplifier circuit 412 comprises n-fet transistors TINP, TINN and TBIAS. Output stage 414 comprises p-fet transistor TNR2, n-fet transistor T2, and inverter circuit 416. Transistors TNR2 and T2 supply an input signal to inverter circuit 416 and the inverter inverts that signal. Differential amplifiers, output stages and inverters are all well known to those skilled in the art, and therefore, no further description is necessary. Common level shifter 404 transitions the output of inverter circuit 416 from VTT to VDD and outputs a signal Z.

[0033] Up-channel receiver 400 is either disabled, enabled during up-channel signaling (e.g. while performing equalization), or enabled during digital scan-based testing. The receiver is disabled when VBIAS is a logic '0'. VBIAS is an inverted version of the PDWN signal as illustrated in Figure 1. When the PDWN signal is active (i.e. logic '1'), VBIAS is pulled to ground and n-fet transistor TBIAS is turned off,

which cuts off the tail bias current IBIAS, thus effectively disabling receiver 400. When PDWN is deactive (i.e. logic '0'), VBIAS is pulled to Vdd and n-fet TBIAS is turned on, thus enabling receiver 400.

[0034] When up-channel receiver 400 is enabled during up-channel signaling, both first built-in offset voltage comparator 408 and second built-in offset voltage comparator 410 are enabled. First built-in offset voltage comparator 408 is enabled when LSSD_EN signal is deactive (logic '0'). Second built-in offset voltage comparator 410 is always enabled because the gate of p-fet transistor TER is tied to ground. In this mode, up-channel receiver 400 outputs a logic '1' at Z when VINP-VINN > Vth+, outputs a logic '0' when VINP-VINN < Vth-, and remains in its previous state when Vth- < VINP-VINN < Vth+. First built-in offset voltage comparator 408 and second built-in offset voltage comparator 410 both have memory, which is desired for improving noise immunity, but not permitted during digital scan-based testing.

[0035] When up-channel receiver 400 is enabled during digital scan-based testing, first built-in offset voltage comparator 408 is disabled and second built-in offset voltage comparator 410 is enabled. First built-in offset voltage

comparator 408 is disabled when LSSD_EN signal is active (logic '1'). By disabling first built-in offset voltage comparator 408, hysteresis is turned off, thus satisfying the digital scan-based methodology requirement of not having memory. When first built-in offset voltage comparator 408 is disabled, second built-in offset voltage comparator 410 functions as a built-in offset-voltage comparator. Therefore, up-channel receiver 400 outputs a logic '1'; if and only if VINP-VINN > Vth+. Due to process, temperature, and supply variation, Vth+ will vary with some range (e.g. Vth+_lower to Vth+_upper). For illustrative purposes, Vth+_lower = 70mV and Vth+_upper = 150mV. This variation in Vth+ is addressed by skewing the output termination impedance as previously described and as illustrated in Figure 3. For illustrative purposes, the output termination impedance at node ZP of Figure 1 is set to 500 Ohms and the output termination impedance at node ZN of Figure 1 is set to 50 Ohms. Thus: a) when a logic '1' is scanned in, if any bit of the differential driver IDAC is on, VINP-VINN will always be greater than Vth+_upper and thus will always guarantee a logic "1" at up-channel receiver output Z; b) when a logic "0" is scanned in, if any bit of the differential driver IDAC is on, VINP-VINN will al-

ways be less than Vth+_lower and thus will always guarantee a logic "0" at up-channel receiver output Z; and c) when all bits of the differential driver IDAC are off, regardless of scanning a logic '1' or logic "0", VINP-VINN is equal to zero (and always less than Vth+_lower) and thus will always guarantee a logic '0' at up-channel output Z. Therefore, the LSB of a differential driver is capable of being digitally tested in a repeatable, predictable, and reliable manner. Alternatively, if up-channel signaling is not required, hysteresis is not needed and only second built-in offset voltage comparator 410 is required.

[0036] Figure 5 illustrates in further detail LSSD test mode control circuit 500, which corresponds to LSSD test mode control circuit 140 of Figure 1. Multiplexer circuits ("MUX") 502, 504, 510 and 512 are controlled by the LSSD_EN signal. When the scan-compatible analog differential driver circuit of the present invention is placed in digital test mode, LSSD_EN is active, thus enabling MUXs 502, 504, 510 and 512 to select test signals for the purpose of digitally testing the driver circuit. During normal operation, LSSD_EN is deactive, thus enabling MUXs 502, 504, 510 and 512 to select signals that correspond to normal functional operation of the driver circuit, which have been pre-

viously described.

[0037] MUX 502 selects either NOMINAL_RESCTRL_P<5:0> or hard-wired value '011111' in response to LSSD_EN. MUX 504 selects either NOMINAL_RESCTRL_N<5:0> or hard-wired value '111101' in response to LSSD_EN. During normal operation, LSSD_EN is deactivate (logic '0') and MUX 502 selects NOMINAL_RESCTRL_P<5:0> and MUX 504 selects NOMINAL_RESCTRL_N<5:0>. As previously described, NOMINAL_RESCTRL_P<5:0> and NOMINAL_RESCTRL_N<5:0> program the output termination impedance so that the impedance matches at nodes ZP and ZN of Figure 1. This occurs when NOMINAL_RESCTRL_P<5:0> = NOMINAL_RESCTRL_N<5:0>. During digital scan-based testing, LSSD_EN is activate (logic '1'). When LSSD_EN is active, MUX 502 selects a hardwired value for RESCTRL_P<5:0> and MUX 504 selects a hardwired value for RESCTRL_N<5:0>. In the preferred embodiment, when LSSD_EN is activate, RESCTRL_P<5:0> is set to '011111' and RESCTRL_N<5:0> is set to '111101'. These values allow the output termination impedance of programmable termination network 120 of Figure 1 to be skewed in accordance with the present invention and as previously described. The values corre-

sponding to RESCTRL_N/P<5:0> may be supplied from any storage element which is accessible during digital testing (i.e. embedded DRAM, fuses, ROM, etc.) so long as those values do not switch during digital testing. Switching of these signals can produce unpredictable test results. OR circuits 506 and 508 are optional and allow leakage testing to be performed by setting RESCTRL_P<5:0> and RESCTRL_N<5:0> to LT which equals '111111'. Leakage testing is well known in the art, and thus, is not discussed in further detail.

[0038] MUX 510 selects the drive strength signal to be supplied to power DAC 280 of Figure 2. During digital scan-based testing, the power to IDAC circuit 270 of Figure 2 is limited so as to not overpower the 3K Ohm resistor components Rn6 and Rp6 of Figure 3. When LSSD_EN is active, MUX 510 selects the hardwired value '0100000' to be TX_POWER<6:0>. This value programs the IDAC circuit of the differential driver as illustrated in Figure 2 to a quarter of the normal operating power. During normal operation, MUX 510 selects NOMINAL_TX_POWER<6:0> to be TX_POWER<6:0>.

[0039] MUX 512 selects either NOMINAL_SEG_DISABLE<7:0> or a decoded signal supplied from decoder 514 in response to

LSSD_EN. During digital testing, only one segment of the differential driver may be tested during a test sequence (e.g. load test patterns, run system clock, unload test results). Test patterns that represent which segment is to be tested during a test sequence are provided to decoder 514 from SRLs 516 during digital testing. Decoder 514 may be any standard 3 to 8 decoder and decodes the signals provided by SRLs 516. For a differential driver that contains eight segments, three SRLs (i.e. 2^3 2^2 2^1) supply test patterns to decoder 514. These three inputs to decoder 514 enable the decoder to provide eight outputs to the differential driver when being tested, each output representing which one of eight segments within the differential driver will be activated during a particular test time. Test patterns are loaded into the SRLs, or "scanned in", each time a different segment is to be tested. For example, when 2^3 2^2 2^1= 0 0 0, SEG_DISABLE<7:0> = <11111110>; when 2^3 2^2 2^1= 0 0 1, SEG_DISABLE<7:0> = <11111101>; when 2^3 2^2 2^1 = 0 1 0, SEG_DISABLE<7:0> = <11111011>; etc.; and finally when 2^3 2^2 2^1 = 1 1 1, SEG_DISABLE<7:0> = <01111111>. The decoded signal is selected by MUX 512 and transmitted to the differential driver when LSSD_EN is

active. During normal operation, MUX 512 selects NOMINAL_SEG_DISABLE<7:0>. The number of SRLs required to provide test input to the decoder and the size of the decoder depend upon the number of segments contained within the differential driver. Thus, any size decoder and number of SRLs for inputting test signals to the decoder are within the scope of this invention. OR circuit 518 is optional and allows the differential driver to be placed in tristate mode when TS is active. Placing a driver in tristate mode is well known in the art, and thus, is not discussed in further detail.

[0040] Logic circuit 520 either inhibits or gates NOMINAL_PDWN signal depending upon the value of LSSD_EN. When in digital scan-based test mode, LSSD_EN is active and inverted to a logic '0' at the input to logic circuit 520, thus inhibiting NOMINAL_PDWN and resulting in PDWN being a logic '0'. This assures that up-channel receiver 130 of Figure 1 remains powered on during digital testing as previously described and as illustrated in Figure 4. During normal operation, the receiver may be powered down by activating the NOMINAL_PDWN signal (i.e. a logic '1'). LSSD_EN does not inhibit NOMINAL_PDWN when LSSD_EN is deactivate. Instead, logic circuit 520 gates NOMINAL_PDWN

when LSSD_EN is deactive.

[0041] Figure 6 illustrates a method of digitally testing differential driver 110 of Figure 1 in accordance with the present invention. Digital scan-based test mode is activated at 600 by activating the LSSD_EN signal illustrated in Figure 1. In the preferred embodiment, this signal is a primary I/O signal that electrically configures the scan-compatible analog differential driver circuit 100 of Figure 1 for digital testing. The LSSD_EN signal adjusts the electrical properties of programmable termination impedance network 120 of Figure 1 at 610 by programming RESCTRL_P<5:0> to '0111111' and RESCTRL_N<5:0> to '111101', thus skewing the output impedance of the programmable termination impedance network in accordance with the present invention and as previously described. The LSSD_EN signal also adjusts the offset voltage of up-channel receiver 130 of Figure 1 and selects a suitable power range for IDAC circuit 270 of Figure 2 at 620 in accordance with the present invention and as previously described. For illustrative purposes, the power to the IDAC circuit is set to a quarter of the normal operating power by setting TX_POWER<6:0> to '0100000' as previously described and as illustrated in Figure 5 so as to not overpower the

3K Ohm resistor components Rn6 and Rp6 of Figure 3. The power range selectable by the LSSD_EN signal is dependent upon the configuration of the programmable termination impedance network and any range selected is within the scope of the invention. Additionally, LSSD_EN also enables decoder 514 of Figure 5 at 630. In accordance with the present invention and as previously described, the decoder activates only one segment of the differential driver during any one test sequence, thus preventing segment contention at the output of the differential driver under test.

[0042] During digital scan-based testing, the decoder determines which segment is to be activated and activates that segment at 640 in accordance with the present invention and as previously described. The differential driver circuit is stimulated from SRLs (e.g. LSSD or GSM) at 650. During digital scan-based test modeling, the differential driver is modeled, for example as a number of n-bit OR gates, and digital test patterns are automatically generated (ATPG) for testing the components of the driver for stuck-at '1' or '0' faults. These test patterns provide stimulus to the driver circuit at 650 during digital scan testing. The stimulus represented by the TX_COEFFx<x:0> signals, which

are generated during ATPG, are stored in SRLs and stimulate the differential driver circuit during digital scan-based testing. The four bits of differential data input signal AP<3:0> as illustrated in Figure 2 are supplied from SRLs. The four bits of differential data input signal AN<3:0> as illustrated in Figure 2 are also supplied from SRLs. The input stimulation signals to the differential driver (TX_COEFFx<x:0>, AP<3:0>, AN<3:0>, TX_POLARITY<3:0>, TAPDIS0/2/3, and SEG_DISABLE<7:0>) will all be observed at the output Z of up-channel receiver 130 of Figure 1, which is connected to a SRL. Thus, the IDACs comprising the differential driver are digitally testable and observable during digital scan testing at 660. Each segment is activated in accordance with the present invention and as previously described and tested until all segments have been tested or until a fail occurs at 670. The LSB of the differential driver is stimulated and observed by stepping through each segment and testing each IDAC input bit. When testing is complete, digital test mode is deactivated at 680 by deactivating the LSSD_EN signal. When LSSD_EN is deactivate, the nominal values for RESCTRL_P/N, TX_POWER, and SEG_DISABLE as illustrated in Figure 5 are supplied to

scan-compatible analog differential driver circuit 100 of Figure 1 in accordance with the present invention and as previously described. Digital scan testing methodologies are well known in the art, in particular, the incorporation of a digital scan architecture into a design, the generation of patterns for testing the design, and the stimulation and observation of circuits within the design.

[0043] In an alternate embodiment, up-channel receiver 130 of Figure 1 is capable of being powered down when not in use. When digital scan-based test mode is activated at 600, NOMINAL_PDWN signal as previously described and as illustrated in Figure 5 is inhibited by LSSD_EN. When LSSD_EN is active, PDWN is a logic '0', thus ensuring that the receiver remains powered on during testing. After testing is complete and digital test mode is deactivated at 680, NOMINAL_PDWN is no longer inhibited by LSSD_EN and may be activated to power down the differential receiver.

[0044] The description of the present invention has been presented for purposes of illustration and description but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art. The

embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.